In response to the objection to claim 29, that claim has been cancelled.

Applicant notes with appreciation the finding that claims 11, 12, 26 and 27 would be allowed if rewritten in independent form. Those claims have been so rewritten and should thus now be allowable.

The remaining claims were rejected under 35 U.S.C. 102 or 103 as being unpatentable over Ben-Michael (EP 0886454A2). It is respectfully submitted that the rejection can not be applied to the amended claims. Ben-Michael relates to a first in first out (FIFO) memory. If on-chip portions of the FIFO are full, bursts of data are forwarded to off-chip memory, but the system continues to operate as a FIFO.

The present invention relates to a system in which data is read from memory in accordance with an arbitration process (page 7, lines 4-14). Accordingly, data stored in the buffer must be randomly accessed. A FIFO as disclosed in Ben-Michael would not be suitable for such a buffer.

In accordance with the present invention as now recited in claims 1, 16, 31 and 40, the first set of buffers operates as a cache with information units being evicted to the secondary set of buffers on other than a first in first out basis. Support for the claim amendments can be found, for example, at page 10, lines 4-6.

In one embodiment as recited in claims 4, 19, 34 and 42, information units are accessed from the buffer pool through a pointer array of pointers pointing, for example, to information corresponding to virtual channels. Ben-Michael does not suggest virtual channels. Further, the only pointers used to identify data are conventional FIFO pointers which identify the single locations into which data is written and from which data is read. Such cannot be considered an array of pointers.

In accordance with another embodiment recited in claims 5-7, 20-22, 35 and 43, the first set of buffers is organized as a set associative cache such as illustrated in Figs. 8 and 9. Ben-Michael teaches only a FIFO, and there is no suggestion of organizing the memory as a set associative cache.

With respect to claims 8-10, 23-25, 36, 37 and 44, though flow control is known in other applications, there is no suggestion in Ben-Michael or in any other reference of using flow control to stop the arrival of new information units while transferring units between the claimed buffers.

Nor is there an suggestion in Ben-Michael or any other reference of the multicomputer or fabric router applications recited in claims 13, 15, 28, 30, 39 and 45.

There is no suggestion of applying concepts presented in Ben-Michael to virtual channels as described, for example, in U.S. Patent 6,285,679, as recited in claims 3, 7, 18, 22, 33, 41 and 46-49.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned at (978) 341-0036.

Respectfully submitted,
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MARKED UP VERSION OF AMENDMENTS

Claim Amendments Under 37 C.F.R. § 1.121(c)(1)(ii)

1. (Twice Amended) A router including buffers, for information units transferred through the router, comprising:

a first set of rapidly accessible buffers which store information units received at an input link; and

a second set of buffers for the information units that are accessed more slowly than the first set[.];

the first set of buffers operating as a cache with information units being evicted to the second set of buffers according to an algorithm other than order of receipt in the first buffer.

11. (Amended) A router [as claimed in claim 1 further comprising] including buffers, for information units transferred through the router, comprising:

a first set of rapidly accessible buffers which store information units received at an input link; [and]

a second set of buffers for the information units that are accessed more slowly than the first set; and

miss status registers to hold information units waiting for access to the second set of buffers.

12. (Amended) A router [as claimed in claim 1 further comprising] including buffers, for information units transferred through the router, comprising:

a first set of rapidly accessible buffers which store information units received at an input link; [and]

a second set of buffers for the information units that are accessed more slowly than the first set; and

an eviction buffer to hold entries staged for transfer from the first set of buffers to the second set of buffers.

16. (Twice Amended) A method of buffering information units in a router comprising:

storing the information units received at an input link in a first set of rapidly accessible buffers; and

storing overflow from the first set of buffers in a second set of buffers that are, accessed more slowly than the first set[.];

the first set of buffers operating as a cache with information units being evicted to the second set of buffers according to an algorithm other than order of receipt in the first buffer.

26. (Twice Amended) A method [as claimed in claim 16 further comprising] of buffering information units in a router comprising:

storing the information units received at an input link in a first set of rapidly accessible buffers; [and]

storing overflow from the first set of buffers in a second set of buffers that are accessed more slowly than the first set; and

storing information units waiting for access to the second set of buffers in miss status registers.

27. (Amended) A method [as claimed in claim 16 further comprising] of buffering information units in a router comprising:

storing the information units received at an input link in a first set of rapidly accessible buffers; [and]

storing overflow from the first set of buffers in a second set of buffers that are accessed more slowly than the first set; and

storing information units staged for transfer from the first set of buffers to the second set of buffers in an eviction buffer.

31. (Twice Amended) A network comprising a plurality of interconnected routers, each router including information unit buffers comprising:

a first set of rapidly accessible information unit buffers which store information units received at an input link; and

a second set of information unit buffers which store the information units and that are accessed more slowly than the first set[.];

the first set of buffers operating as a cache with information units being evicted to the second set of buffers according to an algorithm other than order of receipt in the first buffer.

40. (Twice Amended) A router comprising:

means for storing information units received at an input link in a first set of rapidly accessible buffers; and

means for storing information units in a second set of buffers that are accessed more slowly than the first set[.];

the first set of buffers operating as a cache with information units being evicted to the second set of buffers according to an algorithm other than order of receipt in the first buffer.